1 central processing unit and a direct memory access unit,

2 the interface unit comprising:

3   a receive channel for receiving data groups from the

4 communication bus and the applying the data groups to the

5 ~~data processing unit~~ direct memory access unit; and

6   a transmit channel for receiving data groups from the

7 ~~data processing unit~~ direct memory access unit and applying

8 the signal groups to ~~a~~ the communication bus, wherein the

9 interface unit can function in an ATM interface mode and

10 can function in an I/O interface mode.

11

12 **Please amend Claim 2 as follows.**

13

14   2.   (Currently Amended)   The interface unit as

15 recited in claim 1 wherein the interface unit ~~can function~~

16 ~~is a UTOPIA ATM interface mode and can function in an I/O~~

17 ~~interface mode~~ the direct memory access unit and the

18 central processing unit are fabricated on the same chip.

19

20 **Please amend Claim 3 as follows.**

21

22   3.   (Currently Amended) The interface unit as recited

23 in claim ~~1~~ 2 wherein ~~the interface unit exchanges data~~

24 ~~groups with the direct memory access unit of a~~ the data

25 processing unit includes a plurality of central processing

26 units coupled to the direct memory access unit.

27

28   4.   (Original)   The interface unit as recited in

29 claim 1 further comprising a control register, the control

30 register determining when the interface unit is in the ATM

1   mode of operations and when the interface unit is in the

2   I/O mode of operation.

3

4   5.   (Original)   The interface unit as recited in

5   claim 1wherein the interface unit includes:

6   an input interface unit;

7   an output interface unit;

8   an input buffer memory unit, wherein the transfer

9   between the input buffer memory unit and the direct memory

10   access unit is determined by a receive event signal; and

11   an output buffer memory unit, wherein the transfer

12   between the direct memory access unit and the output buffer

13   memory unit is determined by a transmit event signal.

14

15   6.   (Original)   The interface unit as recited in

16   claim 1 wherein the UTOPIA ATM URDATA signal corresponds to

17   an I/O OUTDATAVALID signal, and wherein a UTOPIA ATM UXCLAV

18   signal corresponds to an I/O INDATAVALID signal.

19

20   **Please amend claim 7 as follows.**

21

22   7.   (Currently Amended) A method of exchanging data

23   groups between a communication bus and a data processing

24   system, the data processing unit including a central

25   processing unit and a direct memory access unit, the method

26   comprising:

27   in response to a first set of signals in an interface

28   unit, exchanging data groups with the communication bus in

29   a ATM mode of operation; and

1   in response to a second set of signals in the

2   interface unit, exchanging data groups <u>with the</u>

3   <u>communication bus</u> in an I/O mode of operation.

4

5   **Please amend Claim 8 as follows.**

6

7   8.   (Currently Amended) The method as recited in

8   claim 7 ~~wherein exchanging data groups includes exchanging~~

9   ~~data groups in a UTOPIA AMT mode of operation~~ <u>further</u>

10 <u>comprising fabricating the interface unit, the direct</u>

11 <u>memory access unit and the central processing unit on a</u>

12 <u>single chip.</u>

13

14   9.   (Original)   The method as recited in claim 8

15 wherein the processor is a digital signal processor.

16

17   10. (Original)   The method as recited in claim 8

18   further comprising implementing the interface unit

19   including:

20   an input interface unit;

21   an output interface unit;

22   an input buffer memory unit, wherein the transfer

23 between the input buffer memory unit and the direct memory

24 access unit is determined by a receive event signal; and

25   an output buffer memory unit, wherein the transfer

26 between the direct memory access unit and the output buffer

27 memory unit is determined by a transmit event signal.

28

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1   **Please amend Claim 11 as follows.**

2

3   11.   (Currently amended) The method as recited in

4   claim 10 further including storing the first and the second

5   set of signals in a control register in the interface unit,

6   the stored signals determining when the interface unit is

7   in the ATM mode or is in the I/O mode.

8

9   **Please amend Claim 12 as follows.**

10

11   12.   (Currently Amended) The method as recited in

12   claim 11 ~~wherein 1~~ wherein the UTOPIA ATM URDATA signal

13   corresponds to an I/O OUTDATAVALID signal, and wherein a

14   UTOPIA ATM UXCLAV signal corresponds to an I/O INDATAVALID

15   signal.

16

17   **Please amend Claim 13 as follows.**

18

19   13.   (Currently Amended) A data processing unit

20   comprising:

21   a connector for coupling to a communication bus;

22   a processor;

23   a direct memory access unit; and

24   an interface unit implementing the exchange of data

25   groups between the connector and the ~~processor~~ direct

26   memory access unit; the interface unit including a control

27   register, the interface unit operating in an ATM mode when

28   a first set of signals are stored in the control register,

29   the interface unit operating in an I/O mode when a second

30   set of signals are stored in the control register.

1   **Please amend Claim 14 as follows.**

2

3   14.   (Currently Amended) The data processing system as

4   recited in claim 13 wherein the interface unit, ~~operates in~~

5   ~~a UTOPIA ATM mode when the first set of signals are stored~~

6   ~~in the control register~~ the direct memory access unit and

7   the processor are fabricated on a single chip.

8

9   15.   (Original)   The interface unit as recited in

10 claim 13, the interface unit including:

11   an input interface unit;

12   an output interface unit;

13   an input buffer memory unit; wherein the transfer

14 between the input buffer memory unit and the direct memory

15 access unit is determined by a receive event signal; and

16   an output buffer memory unit, wherein the transfer

17 between the direct memory access unit and the output buffer

18 memory unit is determined by a transmit event signal.

19

20 **Please amend Claim 16 as follows.**

21

22   16.   (Currently Amended) The data processing unit as

23 recited in claim ~~13~~ 14 wherein the ~~processor~~ data

24 processing unit includes a ~~direct memory access unit, the~~

25 ~~interface unit coupled between the direct memory access~~

26 ~~unit and the connector~~ plurality of processors.

27

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